Figure 1.6 Reduced clock slopes can cause a register circuit to fail.
Figure 1.7  Impact of clock misalignment.
For a current of 100 A, a wire resistance of 1.25 mΩ leads to a 5% drop in supply voltage (2.5 V supply)! On the other hand, current demand can change from zero to this peak value within 1nsec which leads to a current variation of 100GA/sec!
Fundamental Design Metrics

- Functionality
- Scalability
- Cost
  - NRE (fixed) costs - design effort
  - RE (variable) costs - cost of parts, assembly, test
- Reliability, robustness
  - Noise margins
  - Noise immunity
- Performance
  - Speed (delay)
  - Power consumption; energy
- Time-to-market
Cost of Integrated Circuits

- **NRE (non-recurring engineering) costs**
  - Fixed cost to produce the design
    - design effort
    - design verification effort
    - mask generation
  - Influenced by the design complexity and designer productivity
  - More pronounced for small volume products

- **Recurring costs – proportional to product volume**
  - silicon processing (also proportional to chip area)
  - Parts
  - assembly (packaging)
  - test

\[
\text{cost per IC} = \text{variable cost per IC} + \frac{\text{fixed cost}}{\text{volume}}
\]
Die Cost

Single die

Wafer

Going up to 12” (30cm)

From http://www.amd.com
Cost per Transistor

Fabrication capital cost per transistor

<table>
<thead>
<tr>
<th>Year</th>
<th>Cost (¢-per-transistor)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1982</td>
<td>0.10</td>
</tr>
<tr>
<td>1985</td>
<td>0.01</td>
</tr>
<tr>
<td>1988</td>
<td>0.001</td>
</tr>
<tr>
<td>1991</td>
<td>0.0001</td>
</tr>
<tr>
<td>1994</td>
<td>0.00001</td>
</tr>
<tr>
<td>1997</td>
<td>0.000001</td>
</tr>
<tr>
<td>2000</td>
<td>0.0000001</td>
</tr>
<tr>
<td>2003</td>
<td>0.00000001</td>
</tr>
<tr>
<td>2006</td>
<td>0.000000001</td>
</tr>
<tr>
<td>2009</td>
<td>0.0000000001</td>
</tr>
<tr>
<td>2012</td>
<td>0.00000000001</td>
</tr>
</tbody>
</table>
Recurring Costs

variable cost = \frac{\text{cost of die} + \text{cost of die test} + \text{cost of packaging}}{\text{final test yield}}

\text{cost of die} = \frac{\text{cost of wafer}}{\text{dies per wafer} \times \text{die yield}}

\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}}

die yield = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}

die yield (\%) = \frac{\text{No. of good chips per wafer} \times 100}{\text{Total number of chips per wafer}}
\( \alpha \) is a parameter that depends upon the complexity of the manufacturing process and is roughly proportional to the number of masks.

\[ \alpha = 3 \quad \text{(a good estimate for today’s complex CMOS processes)} \]

A value between 0.5 - 1 defects per cm\(^2\) is typical these days.

\[
\text{die cost} = f(\text{die area})^4
\]

- Smaller gate → higher integration density → smaller die size
- Smaller gate → faster
  - less energy
  - less gate capacitance
Yield Example

Example

- wafer size of 12 inches, die size of 2.5 cm², 1 defects/cm², $\alpha = 3$ (measure of manufacturing process complexity)
- 252 dies/wafer (remember, wafers round & dies square)
- die yield of 16%
- $252 \times 16\% = \text{only 40 dies/wafer die yield!}$
## Examples of Cost Metrics (1994)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Defects/cm²</th>
<th>Area (mm²)</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super SPARC</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
Reliability

Noise in Digital Integrated Circuits

- Noise – unwanted variations of voltages and currents at the logic nodes
- from two wires placed side by side
  - capacitive coupling
    - voltage change on one wire can influence signal on the neighboring wire
    - cross talk
  - inductive coupling
    - current change on one wire can influence signal on the neighboring wire
- from noise on the power and ground supply rails
  - can influence signal levels in the gate
Static Gate Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.

- Digital circuits perform operations on Boolean variables $x \in \{0, 1\}$

- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$

- Difference between $V_{OH}$ and $V_{OL}$ is the logic or *signal swing* $V_{sw}$
DC Operation
Voltage Transfer Characteristic

VOH = f(VOL)
VOL = f(VOH)
VM = f(VM)
Mapping between analog and digital signals

“1”

\[ V_{OH} \]

\[ V_{IH} \]

Undefined Region

“0”

\[ V_{IL} \]

\[ V_{OL} \]

\[ V_{out} \]

\[ V_{OH} \]

Slope = -1

\[ V_{OL} \]

\[ V_{IH} \]

\[ V_{IL} \]

Slope = -1

\[ V_{in} \]
Noise Margins

- For robust circuits, want the “0” and “1” intervals to be as large as possible.

\[
\text{Noise Margin High} \quad \text{NM}_H = V_{OH} - V_{IH}
\]

\[
\text{Noise Margin Low} \quad \text{NM}_L = V_{IL} - V_{OL}
\]

Large noise margins are desirable, but not sufficient …
Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise (reject a noise source)

- For good noise immunity, the signal swing (i.e., the difference between $V_{OH}$ and $V_{OL}$) and the noise margin have to be large enough to overpower the impact of fixed sources of noise
Assuming $V_{NM} = V_{SW}/2$

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

Given a set of noise sources, we can derive the minimum signal swing necessary for the system to be operational

$$V_{sw} \geq \frac{2 \sum_i f_i V_{Nfi}}{1 - 2 \sum_j g_j}$$

$f =$ transfer function from noise to signal node  
$V_{Nf} =$ amplitude of noise (fixed) source  
$gV_{SW} =$ Noise proportional to the signal swing
Key Metrics & Reliability Properties

- Noise immunity is the more important metric – the capability to suppress noise sources.
- A gate must be *undirectional*: changes in an output level should not appear at any unchanging input of the same circuit.
  - In real circuits *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs).
- *Output impedance* of the driver and *input impedance* of the receiver.
  - Ideally, the output impedance of the driver should be zero.
  - Input impedance of the receiver should be infinity.
A gate with regenerative property ensures that a disturbed signal converges back to a nominal voltage level.
To be regenerative, the VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.
Fan-In and Fan-Out

- **Fan-out** – number of load gates connected to the output of the driving gate
  
  λ gates with large fan-out are slower

- **Fan-in** – the number of inputs to the gate
  
  λ gates with large fan-in are bigger and slower
The Ideal Inverter

- The ideal gate should have
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.

\[ g = -\infty \]

\[ R_i = \infty \]

\[ R_o = 0 \]

\[ \text{Fanout} = \infty \]

\[ \text{NM}_H = \text{NM}_L = \text{VDD}/2 \]
An Old-time Inverter

$V_{out} (V) = \frac{1}{2} \times V_{in} (V) + 0.5$

$NM_L$

$NM_H$

$V_M$
Delay Definitions

![Diagram of signal propagation with input and output waveforms and questions about propagation delay and signal slopes.]

- **Input waveform** (V_{in})
- **Output waveform** (V_{out})

Questions:
- Propagation delay?
- Signal slopes?
Delay Definitions

Propagation delay

\[ t_p = \frac{t_{pHL} + t_{pLH}}{2} \]
T = 2 \times t_p \times N

2N t_p \gg t_f + t_r
Modeling Propagation Delay

- Model circuit as first-order RC network

\[
v_{\text{out}}(t) = (1 - e^{-t/\tau})V
\]

where \( \tau = RC \)

Time to reach 50% point is
\[
t = \ln(2) \tau = 0.69 \tau
\]

Time to reach 90% point is
\[
t = \ln(9) \tau = 2.2 \tau
\]

- Matches the delay of an inverter gate
Power Dissipation

• Instantaneous power:
  \[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

• Supply line sizing (determined by peak power)

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

• Battery lifetime (determined by average power dissipation)

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_t^{t+T} p(t)dt = \frac{V_{\text{supply}}}{T} \int_t^{t+T} i_{\text{supply}}(t)dt \]

• Packaging and cooling requirements
Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related.

- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors:
  - the faster the energy transfer (higher power dissipation) the faster the gate.

- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant:
  - Power-delay product (PDP) – energy consumed by the gate per switching event: \( P_{av} \times t_p \)

- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is:
  - Energy-delay product (EDP) = PDP \( \times t_p \)
Power and Energy Dissipation

- Two important components: static and dynamic

\[ E \text{ (joules)} = C_L V_{dd}^2 P_{0 \rightarrow 1} + t_{sc} V_{dd} I_{\text{peak}} P_{0 \rightarrow 1} + V_{dd} I_{\text{leakage}} \]

\[ P \text{ (watts)} = C_L V_{dd}^2 f_{0 \rightarrow 1} + t_{sc} V_{dd} I_{\text{peak}} f_{0 \rightarrow 1} + V_{dd} I_{\text{leakage}} \]

\[ P_{DP} = C_L V_{dd}^2 f_{0 \rightarrow 1} t_p \]

\[ E_{0 \rightarrow 1} = \int_{0}^{T} P(t) dt = V_{dd} \int_{0}^{T} i_{\text{supply}}(t) dt = V_{dd} \int_{0}^{T} C_L dV_{out} = C_L \cdot V_{dd}^2 \]

\[ E_{\text{cap}} = \int_{0}^{T} P_{\text{cap}}(t) dt = \int_{0}^{T} V_{out} i_{\text{cap}}(t) dt = \int_{0}^{T} C_L V_{out} dV_{out} = \frac{1}{2} C_L \cdot V_{dd}^2 \]